ABSTRACT

An integrated semiconductor circuit can have memory cells, which can be read by word lines and bit lines. Two mutually adjacent bit lines in each case are connected to inputs of the same signal amplifier. In order to compensate for parasitic capacitors, which arise at thin sidewall insulations between the patterned word lines and adjacent bit line contacts, additional contact structures which lead past the word lines and represent dummy contacts can be provided. The additional parasitic capacitances produced by the dummy contact alter the electrical potential of the respective reference bit line at the signal amplifier like the parasitic capacitances of activated bit lines, as a result of which the measured differential potential can be corrected with respect to the parasitic effects.